

ABSTRACT OF THE DISCLOSURE

A logic portion outputs to a DRAM portion a start address and an end address indicating a memory region where data to be stored is present prior to transition to power down mode having reduced current consumption.

5 In the power down mode, a refresh control unit holds the start address and the end address and controls refresh to be carried out for data only in a region requiring refresh. The power supply of the logic portion is set in off state in the power down mode and accordingly a semiconductor device can consume reduced current while holding data.